

Arm® Musca-B1 Test Chip and Board

Technical Overview



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Release Information

Document History

Issue	Date	Confidentiality	Change
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Web Address

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Conformance Notices

Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity



The system should be powered down when not in use.

It is recommended that ESD precautions be taken when handling development boards.

The board generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the target board
- Reorient the receiving antenna
- Increase the distance between the equipment and the receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Note

It is recommended that wherever possible shielded interface cables be used.

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Preface

This preface introduces the *Arm® Musca-B1 Test Chip and Board Technical Overview*.

It contains the following:

- *About this book* on page 6.
- *Feedback* on page 9.

About this book

This book gives an overview of the Arm® Musca-B1 test chip and board.

Intended audience

This book is written for experienced hardware and software developers to enable low-power, secure *Internet of Things* (IoT) endpoint development using the Musca-B1 test chip and board.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction

This chapter introduces the Musca-B1 test chip and Musca-B1 board.

Chapter 2 Hardware and software

This chapter gives an overview of the Musca-B1 test chip and Musca-B1 board hardware and software.

Appendix A Specifications

See the *Arm® Musca-B1 Test Chip and Board Technical Reference Manual* for information on the Musca-B1 board power supply rails and maximum current loads.

Appendix B Revisions

This appendix describes the technical changes between released issues of this book.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the *Arm® Glossary* for more information.

Typographic conventions

italic

Introduces special terminology, denotes cross-references, and citations.

bold

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`monospace`

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`

Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`

Denotes language keywords when used outside example code.

<and>

Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

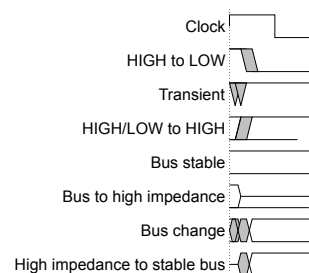


Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW.

Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name, n denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

Arm publications

- *Arm® Musca-B1 Test Chip and Board Technical Reference Manual* (101312).
- *Arm® CoreLink™ SSE-200 Subsystem for Embedded Technical Overview* (101123).
- *Arm® CoreLink™ SSE-200 Subsystem for Embedded Technical Reference Manual* (101104).
- *Arm® CoreLink™ SIE-200 System IP for Embedded Technical Reference Manual* (DDI 0571).
- *Arm® Cortex®-M System Design Kit Technical Reference Manual* (DDI 0479).
- *Arm® Cortex®-M33 Processor Technical Reference Manual* (100230).
- *PrimeCell UART (PL011) Technical Reference Manual* (DDI 0183).
- *Arm® PrimeCell Real Time Clock (PL031) Technical Reference Manual* (DDI 0224).
- *CoreSight™ Components Technical Reference Manual* (DDI 0314).
- *Arm® DS-5 Arm DSTREAM User Guide* (DUI 0481).
- *Arm® DS-5 Using the Debug Hardware Configuration Utilities* (DUI 0498).

The following confidential books are only available to licensees or require registration with Arm.

- *Arm® CryptoCell-312 Technical Reference Manual* (100774).
- *Arm® CryptoIsland-300 Technical Reference Manual* (101119).
- *Arm® v7-M Architecture Reference Manual* (DDI 0403).
- *Arm® AMBA® 5 AHB Protocol Specification* (IHI 0033).
- *Arm® AMBA® APB Protocol Specification Version 2.0* (IHI 0024).

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to errata@arm.com. Give:

- The title *Arm Musca-B1 Test Chip and Board Technical Overview*.
- The number 101311_0000_01_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

————— **Note** —————

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Chapter 1

Introduction

This chapter introduces the Musca-B1 test chip and Musca-B1 board.

It contains the following sections:

- *1.1 Precautions* on page 1-11.
- *1.2 About the Musca-B1 test chip and board* on page 1-12.
- *1.3 Location of components* on page 1-13.

1.1 Precautions

This section describes precautions that ensure safety and prevent damage to your Musca-B1 board.

This section contains the following subsections:

- [1.1.1 Ensuring safety on page 1-11.](#)
- [1.1.2 Operating temperature on page 1-11.](#)
- [1.1.3 Preventing damage on page 1-11.](#)

1.1.1 Ensuring safety

The Musca-B1 board operates at 5V supplied through the DAPLink 5V USB connector.

———— **Warning** ————

Do not use the Musca-B1 board near equipment that is sensitive to electromagnetic emissions, for example, medical equipment.

—————

1.1.2 Operating temperature

The Musca-B1 board has been tested in the temperature range 15°C-30°C.

1.1.3 Preventing damage

The Musca-B1 board is intended for use within a laboratory or engineering development environment.

———— **Caution** ————

To avoid damage to the Musca-B1 board, observe the following precautions:

- Never subject the board to high electrostatic potentials. Observe *ElectroStatic Discharge* (ESD) precautions when handling any board.
 - Always wear a grounding strap when handling the board.
 - Only hold the board by the edges.
 - Avoid touching the component pins or any other metallic element.
 - Do not fit an Arduino Expansion Shield while the Musca-B1 board is powered up.
-

1.2 About the Musca-B1 test chip and board

The Musca-B1 board is a development system that demonstrates the foundation of single-chip secure *Internet of Things* (IoT) endpoints.

Purposes of the Musca-B1 test chip and board

The Arm Musca-B1 board provides access to the Arm Musca-B1 test chip that implements the Arm CoreLink SSE-200 Subsystem for Embedded product.

Major components and systems

The system enables development and evaluation of custom software on the Musca-B1 test chip. The board and Musca-B1 test chip provide the following main features:

- Musca-B1 test chip that includes, but is not limited to, the following:
 - CoreLink SSE-200 subsystem that contains two Arm Cortex-M33 processors.
 - Peripheral and Arduino Expansion Shield interfaces.
- On-board DAPLink that provides the following access:
 - *Serial Wire Debug* (SWD).
 - *USB Mass Storage Device* (USBMSD) for uploading new firmware.
 - USB serial port. The UART on the Musca-B1 test chip does not support hardware flow control.
 - Remote reset.
- On-board:
 - 3-axis orientation and motion sensor (gyro sensor).
 - Temperature sensor/ADC/DAC.
 - *Quad Serial Peripheral Interface* (QSPI) 8MB boot flash.
 - *Secure Digital I/O* (SDIO) microSD card.
- P-JTAG processor debug, 4-bit trace, and SWD header.
- User RGB LED, status LEDs, user reset, and ON/OFF push buttons.
- The board is powered from USB 5V power or Li-ion rechargeable battery backup, battery not supplied, selectable by a slider switch.
- Headers for Arduino Expansion Shield to support development of custom designs:
 - 16 3V3 GPIO.
 - UART. No hardware flow control.
 - SPI, master only.
 - I²C, master only.
 - I²S three-channel, master only.
 - 3-channel *Pulse Width Modulation* (PWM).
 - 6-channel analog interface from the on-board combined ADC, DAC, and GPIO.

Electrical specifications

See the *Arm® Musca-B1 Test Chip and Board Technical Reference Manual* for information on the Musca-B1 board power supply rails and maximum current loads.

1.3 Location of components

The following figure shows the physical layout of the upper face of the Musca-B1 board.

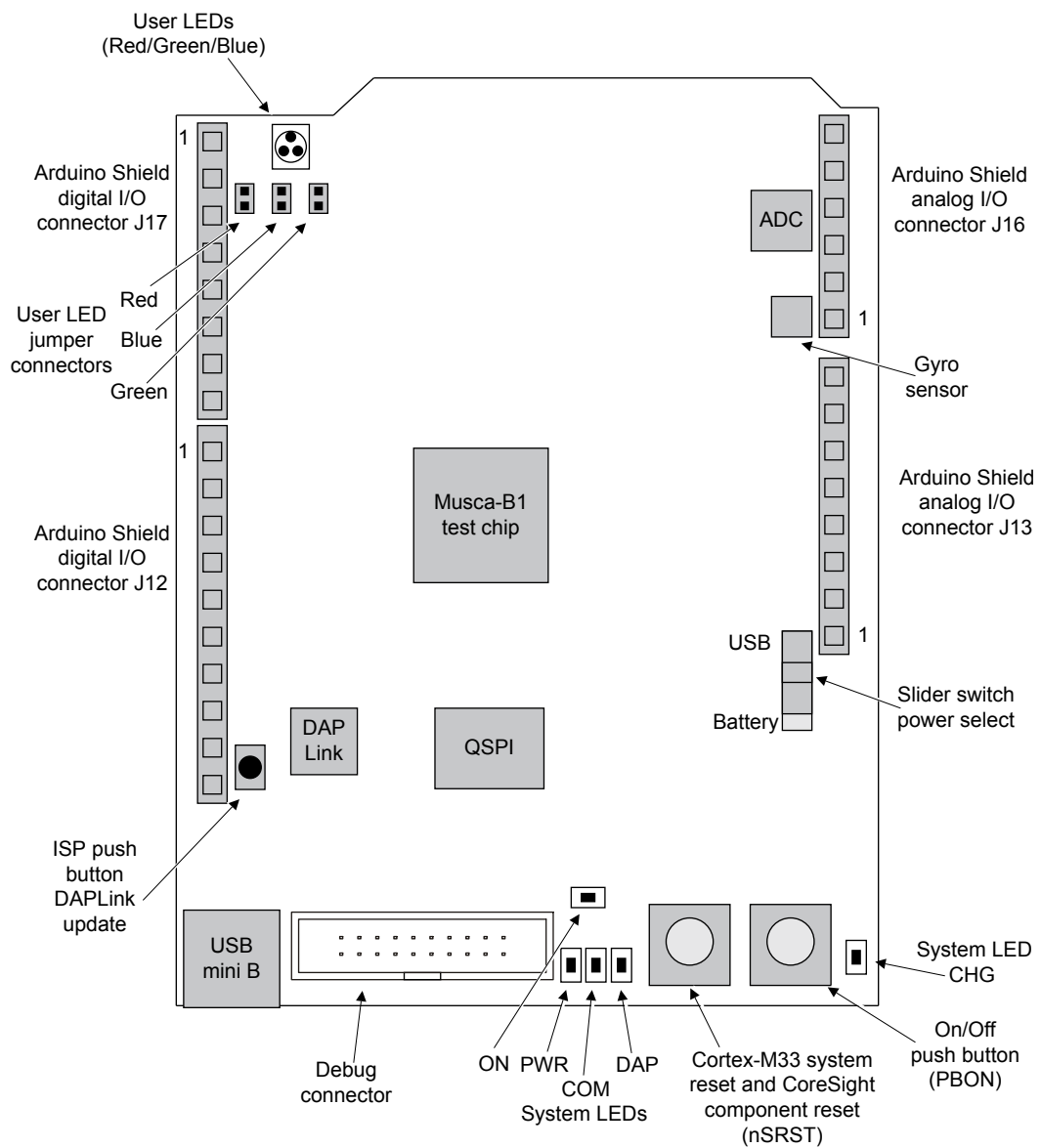


Figure 1-1 Layout of the upper face of the Musca-B1 board

The following figure shows the physical layout of the lower face of the Musca-B1 board.

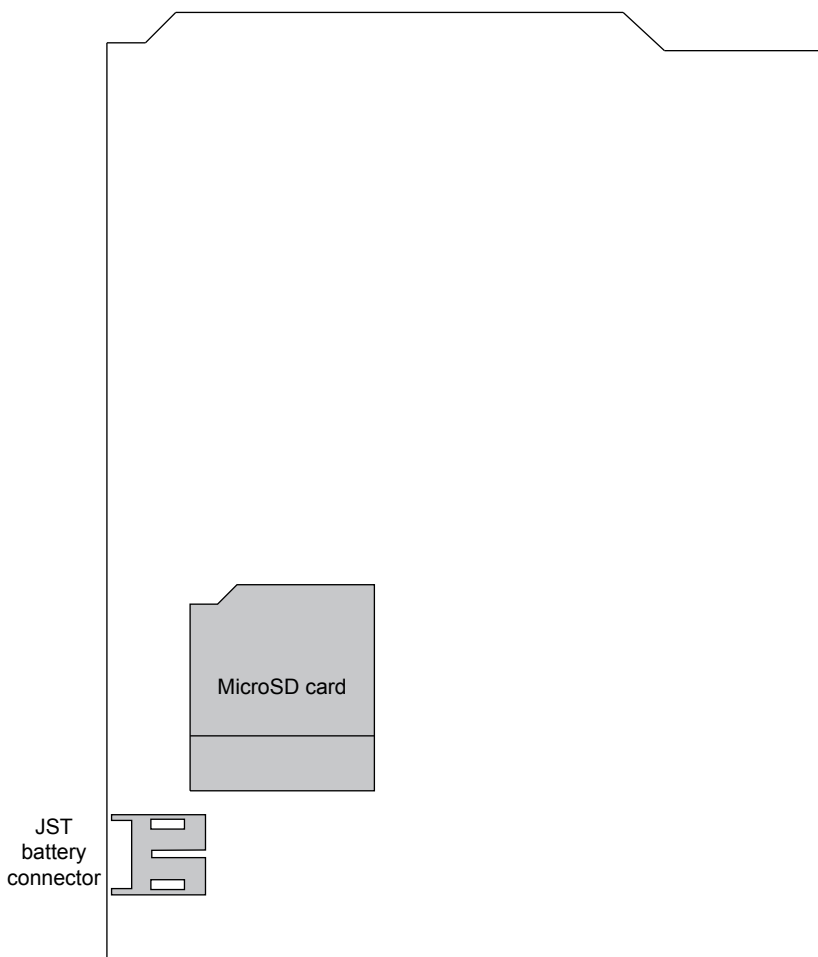


Figure 1-2 Layout of the lower face of the Musca-B1 board

Chapter 2

Hardware and software

This chapter gives an overview of the Musca-B1 test chip and Musca-B1 board hardware and software.

It contains the following sections:

- [2.1 Board hardware on page 2-16.](#)
- [2.2 Musca-B1 test chip on page 2-18.](#)
- [2.3 Software, firmware, board, and tools setup on page 2-22.](#)

2.1 Board hardware

The hardware infrastructure of the Musca-B1 board provides access to the Musca-B1 test chip and supports Shield expansion.

Overview of the Musca-B1 board hardware

The Musca-B1 test chip interfaces connect directly between the test chip and the peripheral devices on the board, and between test chip and the Shield header.

The following figure shows the hardware infrastructure of the Musca-B1 board.

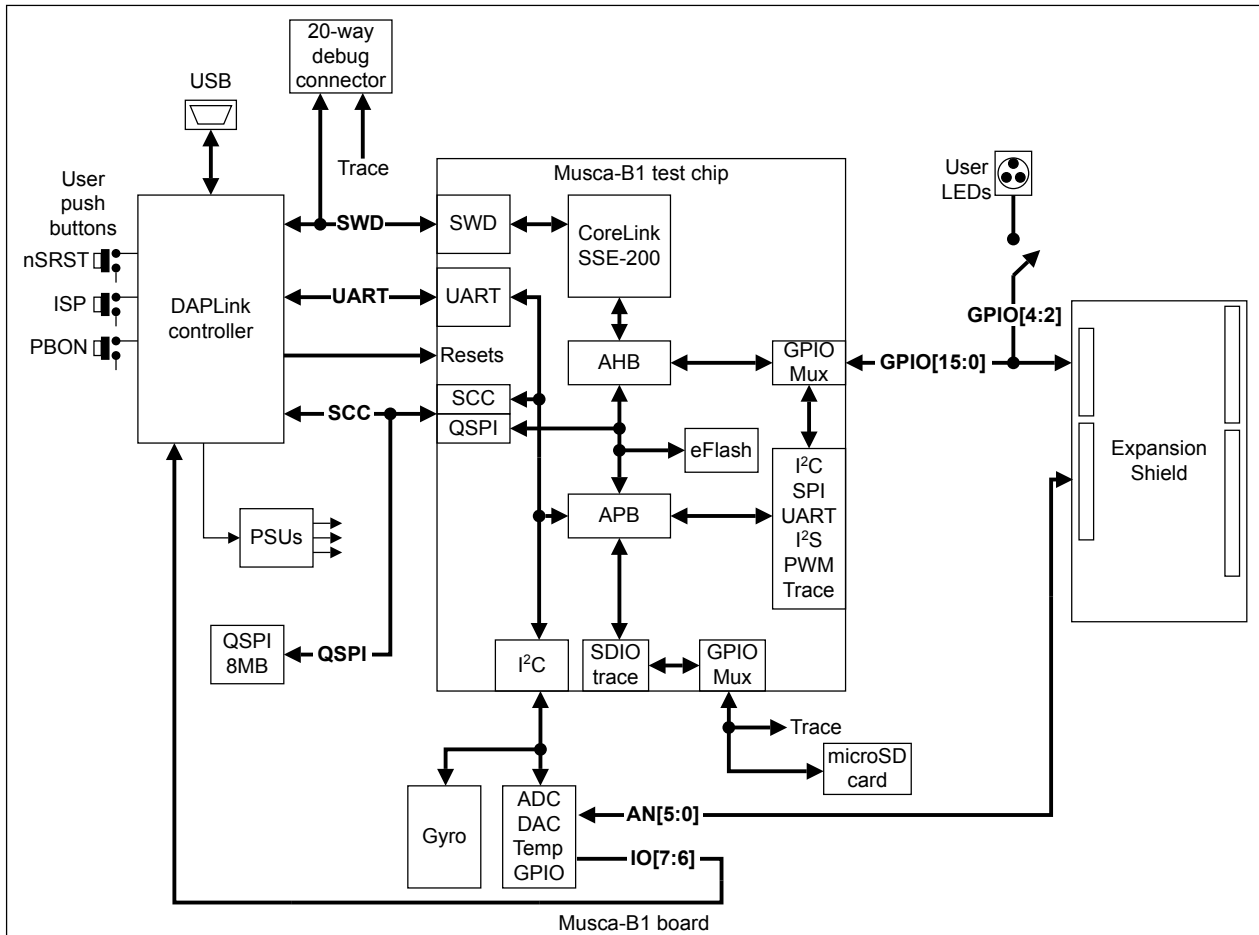


Figure 2-1 Hardware infrastructure of the Musca-B1 board

Musca-B1 board components and systems

The Musca-B1 board contains the following components and systems:

- One Musca-B1 test chip that contains a CoreLink SSE-200 Subsystem for Embedded. The SSE-200 subsystem includes, but is not limited to, the following:
 - CPU0: One Cortex-M33 processor. *Floating Point Unit* (FPU), DSP, no coprocessor.
 - CPU1: One Cortex-M33 processor. FPU, DSP, no coprocessor.
 - Two 2KB instruction caches, one for each processor.
 - 4 × 128KB SRAM. One bank of SRAM functions as *Tightly-Coupled Memory* (TCM), Tightly-Coupled to CPU1.

- CryptoCell-312.
- Timer, Watchdog peripherals, and system control.
- Arduino Shield expansion to enable custom designs by providing the following interfaces:
 - UART. The UART on the Musca-B1 test chip does not support hardware flow control.
 - I²S, three-channel, master only.
 - SPI, master only.
 - I²C, master only.
 - PWM.
 - 6-channel analog interface from the on-board combined ADC, DAC, and GPIO.
 - 16 3V3 GPIO.
- On-board DAPLink that enables the following functionality over USB:
 - *Serial Wire Debug* (SWD).
 - *USB Mass Storage Device* (USBMSD) for uploading new firmware.
 - USB serial port. The UART on the Musca-B1 test chip does not support hardware flow control.
 - Remote reset.
- On-board gyro sensor:
 - MMA7660FC 3-axis orientation and motion detection sensor.
 - I²C interface to Musca-B1 test chip.
- On-board combined ADC/DAC/temperature sensor:
 - AD5593.
 - 6-channel 3V3 ADC/DAC/GPIO interface to Arduino Shield.
 - Temperature indicator.
- Programmable boot select:
 - 512KB on-chip system memory SRAM.
 - 8MB On-board QSPI boot flash.
 - Two 2MB on-chip boot eFlash.
 - Both Secure and Non-secure access.
- Debug connector that provides access to:
 - P-JTAG processor debug.
 - *Serial Wire Debug* (SWD).
 - 4-bit trace.
- User push-button:
 - PBON On/Off push-button.
 - nSRST: Cortex-M33 system reset and CoreSight component reset.
 - ISP: Updates DAPLink firmware.
- RGB LED. Jumper connectors provide optional connections between the Arduino Expansion header and the Musca-B1 test chip:
 - Red LED connected to GPIO[2] pin, optional PWM0.
 - Green LED connected to GPIO[3] pin, optional PWM1.
 - Blue LED connected to GPIO[4] pin, optional PWM2.
- Status LEDs.
- 5V USB or battery power, selectable by slider switch:
 - DAPLink 5V USB connector.
 - CLN 523450, Lithium Ion, 3.7V, 950mAh (not supplied).

See *Arm® Musca-B1 Test Chip and Board Technical Reference Manual* for more information on the Musca-B1 board components and systems.

2.2 Musca-B1 test chip

The Musca-B1 test chip is based on the SSE-200 subsystem which features two Cortex-M33 processors.

Overview of the Musca-B1 test chip

The Musca-B1 test chip features a memory system, integrated connectivity, sensor interfaces, a clock generator, and *Serial Configuration Control* (SCC) registers for setting default powerup values.

See the following documentation for more information on the SSE-200 subsystem:

- *Arm® CoreLink™ SSE-200 Subsystem for Embedded Technical Overview.*
- *Arm® CoreLink™ SSE-200 Subsystem for Embedded Technical Reference Manual.*

See the *Arm® Musca-B1 Test Chip and Board Technical Reference Manual* for more information.

The following figure shows a high-level view of the architecture of the Musca-B1 test chip.

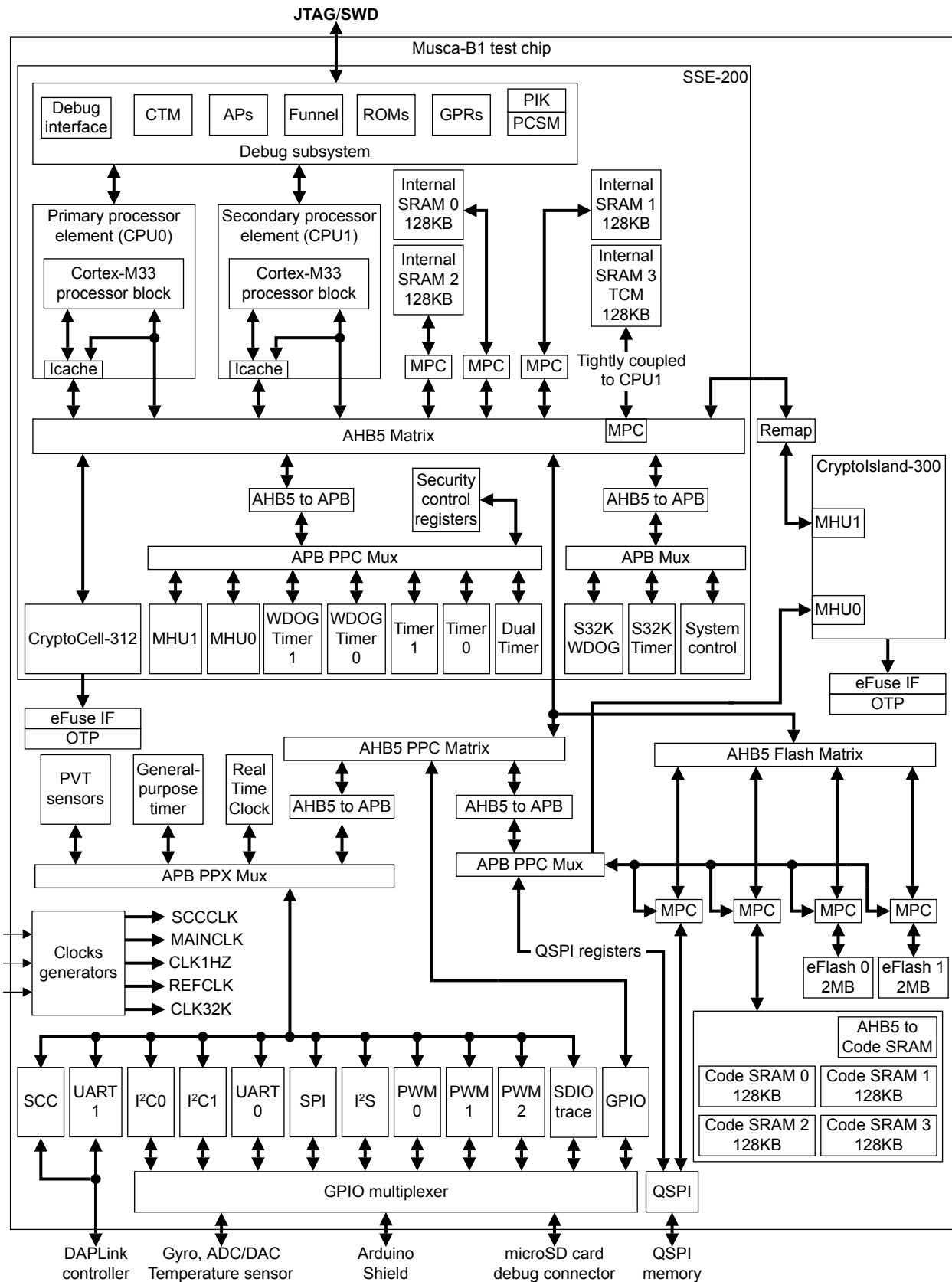


Figure 2-2 Musca-B1 test chip

Major components and systems of the Musca-B1 test chip

SSE-200 subsystem

- Two processors:
- Two Cortex-M33 processors with FPU and DSP, and with no coprocessor:
 - CPU0: 40.96MHz maximum. Used as main processor.
 - CPU1: 163.84MHz maximum.
- Memory system:
 - One 2KB instruction cache for each Cortex-M33 processor.
 - 4 × 128KB SRAM. One bank of SRAM functions as *Tightly-Coupled Memory* (TCM), Tightly-Coupled to CPU1.
- CoreSight components, 4-bit trace, *Cross Trigger Interface* (CTI), and *Serial Wire Debug* (SWD).
- Secure AMBA interconnect:
 - AHB5 Bus matrix.
 - AHB5 *Exclusive Access Monitors* (EAMs).
 - AHB5 *Access Control Gates* (ACGs).
 - AHB5 to APB bridges.
 - Expansion AHB5 master and slave buses - two of each.
- Security components:
 - AHB5 TrustZone® *Memory Protection Controllers* (MPCs).
 - AHB5 TrustZone *Peripheral Protection Controllers* (PPCs).
 - CryptoCell-312.
 - *Implementation defined Attribution Unit* (IDAU).
 - Secure and Non-secure configurable peripherals and memory access.
- Secure APB peripherals:
 - One general-purpose timer with configurable security in the **S32KCLK** domain.
 - Two general-purpose timers, Timer0 and Timer1 with configurable security, in the **SYSCLK** domain.
 - One *Cortex®-M System Design Kit* (CMSDK) dual timer with configurable security.
 - One secure watchdog in the **S32KCLK** domain.
 - One secure watchdog in the **SYSCLK** domain.
 - One Non-secure watchdog in the **SYSCLK** domain.

Musca-B1 test chip outside the SSE-200 subsystem

- One CryptoIsland-300 subsystem, a security enclave module used for Secure access control.
 - 64KB RAM.
- Two 2MB *Embedded Flash* (eFlash) memories.
- 512KB Code SRAM: $4 \times 128\text{KB}$ independently power-enabled.
- Two 8KB true *One-Time Programmable* (OTP) memories:
 - One used for CryptoCell-312.
 - One used for CryptoIsland-300 secure enclave.
- One *Real Time Clock* (RTC) in the Always ON domain.
- One 32-bit general-purpose timer running at 32.768kHz with programmable interrupts.
- 16 external GPIO interrupts.
- 16 GPIO.
- Nine *Process, Voltage, and Temperature* (PVT) sensors:
 - 501-stage ring oscillators that perform boot time process measurements. Software can read data from the sensors in the sensor peripheral and group registers.
- Three-channel I²S:
 - Two master transmitters.
 - One master receiver.
- Three independent *Pulse Width Modulation* (PWM) outputs.
- Two UARTs, UART0 user, UART1 debug. The UART on the Musca-B1 test chip does not support hardware flow control.
- Two I²C:
 - I²C0. Master only.
 - I²C1. Master only to on-board interfaces.
- One SPI master interface.
- One microSD card I/O (SDIO 3.0):
 - Interface width of 4.
 - Up to SDR50.
 - No DMA support.
- One alternate function I/O multiplexer.
- One QSPI for external flash control with *Execute in Place* (XIP) capability.
- Programmable boot select:
 - eFlash 0 or eFlash 1.
 - Code SRAM.
 - External QSPI Flash.
- External powerup reset.
- Three system clock sources:
 - External **REFCLK**, 32.768kHz.
 - External **FASTCLK**, 24MHz.
 - On-chip PLL. Input 32.768kHz. Output up to 40.96MHz to primary processor, CPU0, and 163.84MHz to secondary processor, CPU1.
 - One JTAG/SWD debug port.
- One *Serial Configuration Controller* (SCC) with dual access port:
 - SCC serial during reset.
 - APB after reset.

2.3 Software, firmware, board, and tools setup

Arm supplies software and firmware for the Musca-B1 board.

You can access software and firmware at the Arm Community pages which are accessible from <https://www.arm.com/musca>.

Setting up a project

To power the board, connect the USB port to your computer and press the PBON user push button. The DAPLink interface appears in the Windows device manager as an Mbed™ composite device, part of which is the Mbed serial port, UART. The following figure shows an example configuration that contains the Mbed composite device and the Mbed serial port.



Figure 2-3 DAPLink interface

Note

Other components of the Mbed composite device are not visible in the Windows device manager. See [2.1 Board hardware on page 2-16](#) for the other components of the Mbed composite device.

The UART on the Musca-B1 test chip does not support hardware flow control.

Updating DAPLink firmware

You can update the DAPLink firmware for either QSPI or eFlash. To update the DAPLink firmware, you can use the DAPLink drag and drop update method:

1. Press and hold the ISP button while powering up the board using the USB lead.
2. Delete the `firmware.bin` file that appears in the CRP DISABLD USB drive.
3. Copy `DAPLink_QSPI_XTAL_vxx.bin` or `DAPLink_eFLASH_XTAL_vxx.bin` to the CRP DISABLD drive.

- From a Windows system, you can simply Drag and Drop the file.
- On Linux/Mac OS, use the following command:

```
dd if={new_firmware.bin} of=/Volumes/CRP\ DISABLD/firmware.bin conv=notrunc
```

4. Power cycle the board using the USB lead. Do not press the ISP button during the power cycle.

Updating the application software image

To update the application image, perform the following steps:

1. Power up the board by connecting the USB lead and pressing the PBON button.
2. Drop a .bin format software image onto the MBED drive, for example `blinky.bin`.
3. Power cycle the board or press the nSRST button to reset the system and boot from the new QSPI or eFlash software image.

Note

The file `blinky.bin` is available at the Arm Community pages which are accessible from <https://www.arm.com/musca>.

DAPLink UART setting

The default DAPLink UART setting is 115,200 baud (8N1).

Appendix A

Specifications

See the *Arm® Musca-B1 Test Chip and Board Technical Reference Manual* for information on the Musca-B1 board power supply rails and maximum current loads.

Appendix B

Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following section:

- [B.1 Revisions on page Appx-B-26.](#)

B.1 Revisions

The following table lists the technical changes between released issues of this book.

Table B-1 Issue 101311_0000_00

Change	Location	Affects
No changes, first release.	-	-

Table B-2 Differences between issue 101311_0000_00 and issue 101311_0000_01

Change	Location	Affects
Added CryptoIsland-300 RAM size.	2.2 Musca-B1 test chip on page 2-18	All board versions
Corrected CPU0 and CPU1 maximum operating frequencies.	2.2 Musca-B1 test chip on page 2-18	All board versions
Added information on how to update DAPLink firmware from a Linux/Mac OS.	2.3 Software, firmware, board, and tools setup on page 2-22	All board versions